

Output Settings... Vout

- Displays **Loop A** or **Loop B** information
- 3 tabbed dialogs for each loop
- Active tab is highlighted in bold blue text font
 - Screenshot has **Loop A** and **Vout** information displayed

VID Table

- Selection of VID voltage step

Vboot

- Boot voltage

For Intel application, **VID Table** and **Vboot** can be changed in the [SVID](#) dialog

For AMD application, **VID Table** is automatically changed to 6.25mV

For POL/Telcom or PWM-VID application, **VID Table** and **Vboot** can be change in this tabbed dialog

Slew Rate

- Rate on how fast voltage changes
- For Intel application, Slew Rates can be changed in the [SVID](#) dialog

PMBus Configuration

- Opens the PMBus Configuration dialogue that is use to send PMBus commands to set Vout.

Loadline Settings

Slope

- Use to define how much Vout is adjusted by load current

Offset

- Use to position the Vout with a fixed offset over the all load currents
- Typical value is 0mV

Change Vout

- Manual control of Vout

High Byte (Offset)

- Adds an offset to existing Vout
- Values >80 count converts to a negative number

Low Byte (VID Code)

- Sets a VID code for a specific Vout
- Any settings that is not 0 will override other voltage commands

Output Settings... Vout Protection

Enable detection (Fixed OOVp)

- Enable/disable Fixed OOVp Threshold detection

Fixed OOVp Threshold

- Threshold that determines if Vout is over voltage
- Triggered when $V_{out} > \text{Fixed OOVp Threshold}$
- Always active after the initialization state except during open sense line fault detection
- Recommended setting is $< \text{output cap rating}$ and $> V_{out_Max}$

Enable detection (Tracking OOVp)

- Enable/disable tracking OOVp Threshold detection

Tracking OOVp Threshold

- Threshold is based on the difference between Vout and Vtarget.
- Triggered when $(V_{out} - V_{target}) > \text{Tracking OOVp threshold}$
- Enabled during soft start, calibration, active regulation and shutdown states
- Disabled during DVID ramping
- Recommended setting is 0.4V

OOVp Response

- Response when Vout exceeded any of the fixed or tracking OOVp threshold and when any of the OOVp enable detection is enabled
- Response time: flagged on 4 consecutive samples at a rate of 50MHz are over the threshold

Enable detection (Fixed OUVp)

- Enable/disable Fixed OUVp Threshold detection

Fixed OUVp Threshold

- Output under-voltage protection
- Triggered when $V_{out} < \text{Fixed OUVp Threshold}$
- Only enabled during the active regulation state
- Recommended setting is $< \text{system required min Vout}$ and $> \text{fixed OUVp disable threshold}$

Enable detection (Tracking OUVp)

- Enable/disable tracking OUVp Threshold detection

Tracking OUVp Threshold

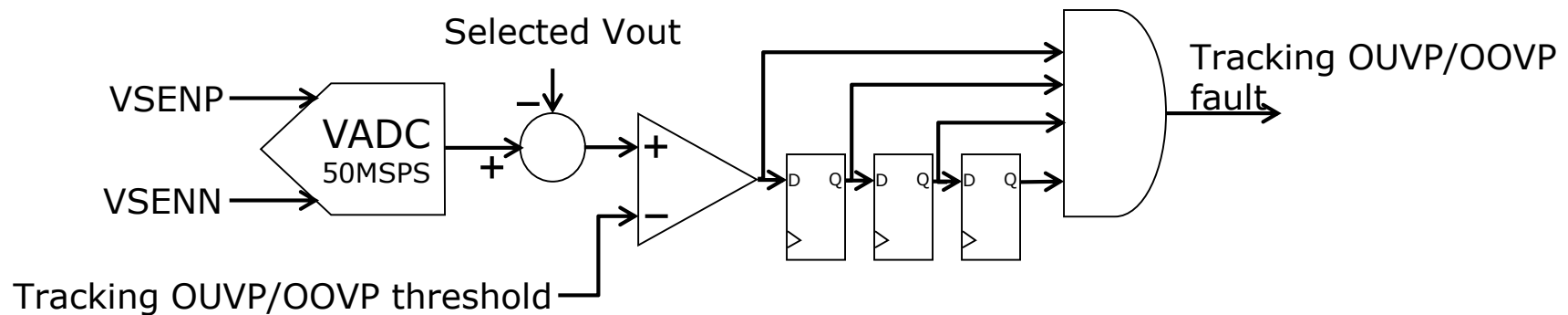
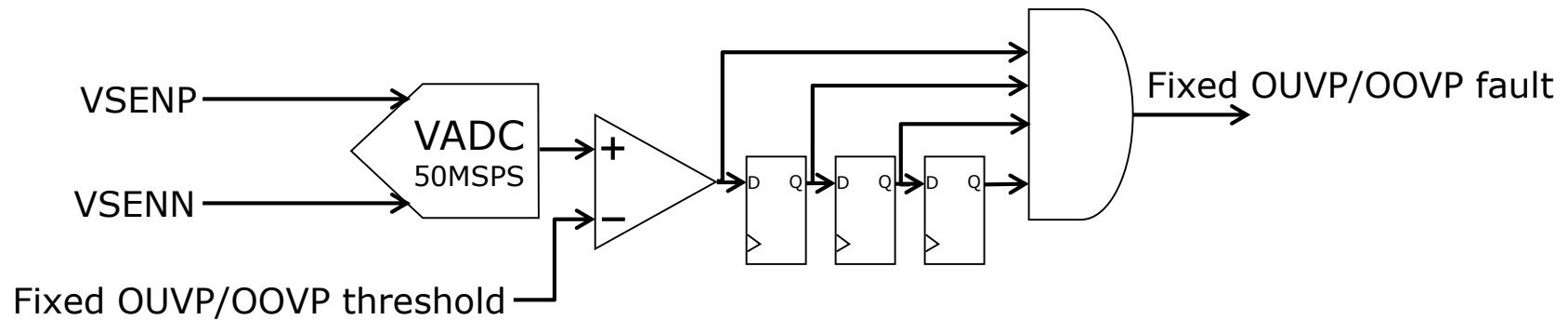
- Triggered when $(V_{target} - V_{out}) > \text{Tracking OUVp threshold}$
- Only enabled during the active regulation state
- Recommended setting is 0.3V

OUVp Response

- Response when Vout exceeded any of the fixed or tracking OUVp threshold and when any of the OUVp enable detection is enabled
- Response time: flagged on 4 consecutive samples at a rate of 50MHz are over the threshold

Output Settings...

Fixed/Tracking OOVp/OUVP fault



4 consecutive samples over/under the limit will trigger the fault.

Output Settings... Vout Protection

HSS Response

- Response on high side short fault (i.e. High side MOSFET is shorted and Vout is raising by itself)
- Input: phase current sampled at 50Mhz rate
- Default threshold: $1.6 \times P2CL$
- Response time: 80ns; 4 consecutive samples at 50Mhz rate greater than threshold

Driver Fault Response

- Response on driver fault signal from power stages
- Input: Tmon Voltage signal
- Detection is enabled all the time
- If Tmon voltage is higher than 2V, a **Driver Fault** will be reported
- Response time:
 - Tmon have to be high for minimum 200ns before fault is flagged
 - Shutdown response at 60ns after fault is flagged

Output Settings - 0x7C

Loop A | Loop B

Vout | **Vout Protection** | Iout Protection

OOVP

Fixed OOVP Threshold: 3.45V ☒ Enable detection

Tracking OOVP Threshold: 0.4V ☒ Enable detection

OOVP Response: Latch

OUVP

Fixed OUVP Threshold: 0.5V ☒ Enable detection

Tracking OUVP Threshold: 0.3V ☒ Enable detection

OUVP Response: Latch

HSS Response: Latch

Driver Fault Response: Latch

Cat Fault Response: Ignore

Write to device | Read from device | Close | ?

Cat Fault Response

- Response on catastrophic fault

Output Settings... Iout Protection

Note: The different thresholds for OCP and warning have an relationship and GUI may limit or round possible settings and change the other limits to match.

Inst. OCP (Over Current Protection)

- This looks at the instant peak current in each phase
- There is a 5 switching cycles delay before any action is taken
 - See next page for diagram
- Response** will determine what action to take when the instant peak current exceeded its limit

Avg OCP (Over Current Protection)

- This looks at the average current in each phase
- Recommended settings per ph:
 - $I_{cc\ Max} * 1.15 / N_{ph\ Max}$
- Response** will determine what action to take when the average current exceeded its limit

OC Warning (Over Current)

- This looks at the average filtered current in each phase
- Fault will be triggered if the average filtered current exceeded this limit

The function Peak Current Control in Sequoia that can be selected can be set to either cycle average that is the same as Sierra or instant current which is a faster but noisier detection mode

Total threshold

- Threshold that represents the total output current where the warning will be triggered

OC warning (PCC in AMD applications)

- A fast lightly filtered Over Current warning signal. Filter can be selected for how long over current have to be before it activates the output. The output can be selected for how long it will stay on after detection. It will reset itself after selected time if no more OC is detected.
- It uses the same threshold current as set in OC warning.

Max Current Digitized

- Highest phase current that can be measured
- Can be changed in the [Current Sense](#) dialogue

Inductance

- Output inductor for the buck converter that can be edited in the [Feedback Loop/Output Model](#) dialogue
- Use in the calculation for the P2CL function

P2CL (Pulse to Pulse Cycle Limit)

- Per phase current limit designed to prevent inductor saturation by monitoring peak inductor current per phase and limit PWM pulse width cycle by cycle
- Recommended value is I_{sat} @ 125 deg C in inductor datasheet minus 1 or 2A.
- Response** will be triggered if current exceeded this limit for 255 consecutive switch pulses

Negative Current Limit (NCL)

- If the current in one phase goes too much negative, its PWM output will go to High Impedance (Hi-Z) for a specified minimum time.
- This function can be enabled by marking the box next to Enable. See explanation on following pages for function

Threshold @ vout=1.76V

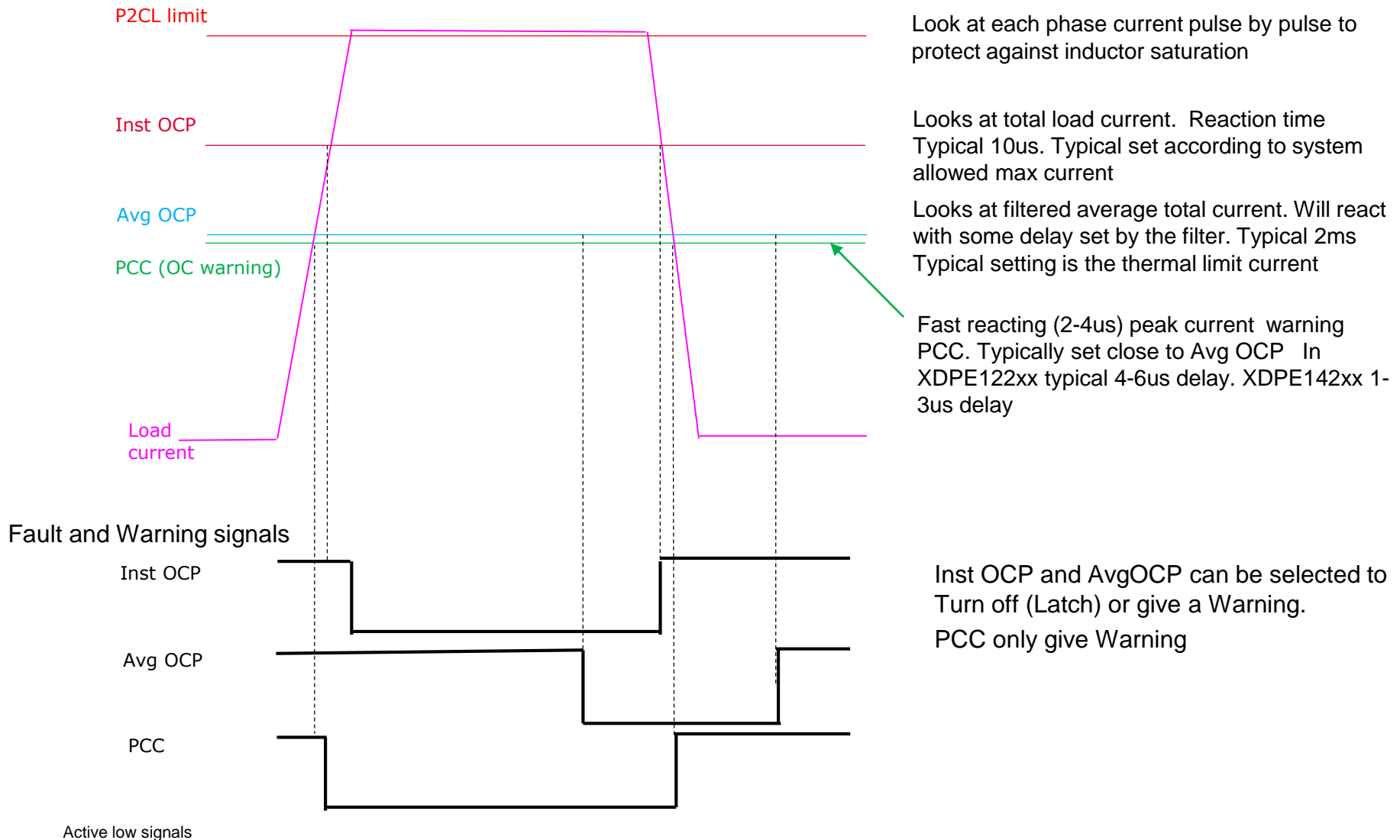
- Maximum difference in phase current to trigger a phase fault. It change a little depending on Vout.

Response

- Response when phase fault signal comes from power stage

Output Settings...

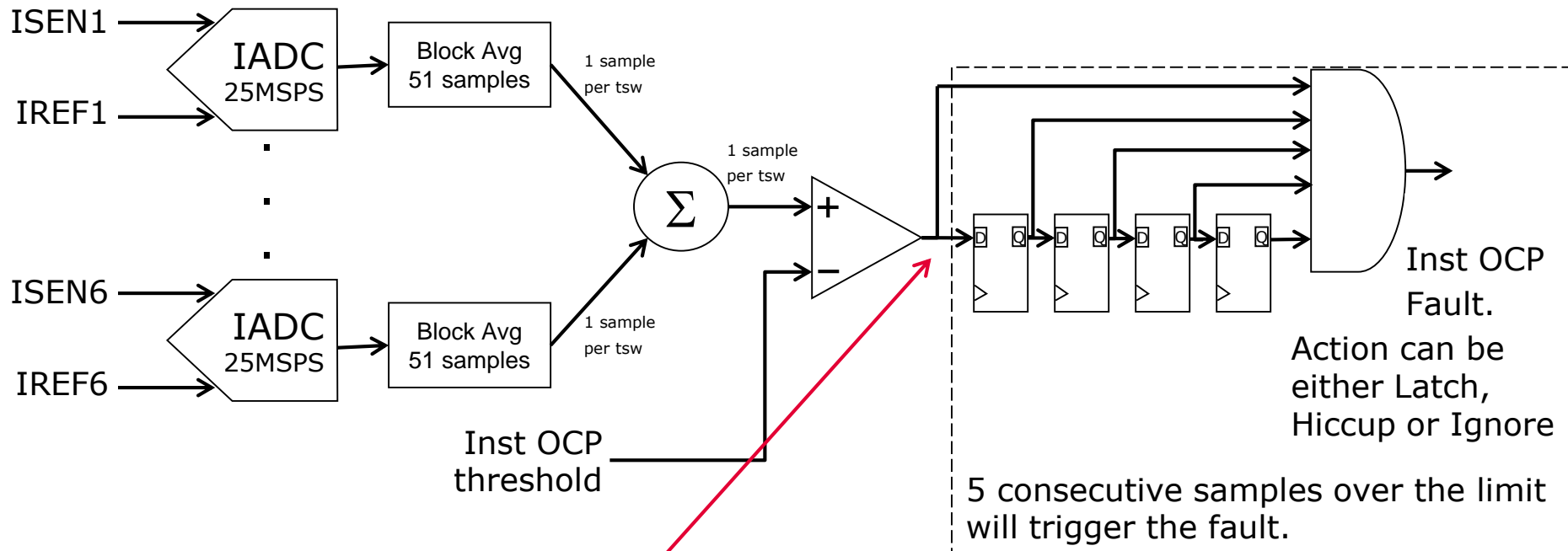
The different current limits in Sequoia/Sierra



Output settings...

Inst OCP behavior

Notice that the current measured is the inductor current and not the direct load current. Inductor current rises slower than the load current and will add a delay that depends on variables like Inductance, Input voltage, output voltage and more.

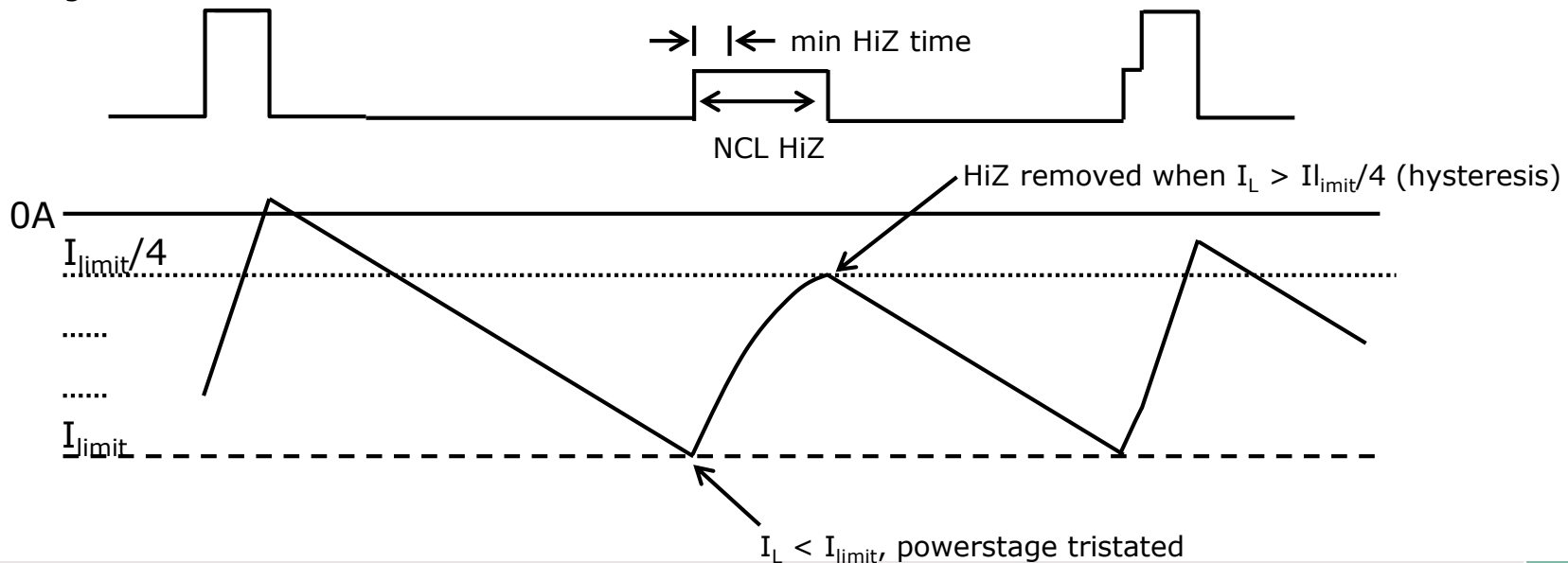


If any sample is under the threshold the Inst OCP flag/fault and timer will reset immediately

Output Settings...

NCL function explanation

- › Input: I_{out}
- › Response time: 5ns; No shutdown response available
- › Recommended settings: amplitude should be greater than the negative current induced by C_{dv}/dt during DVID down.
- › Shutdown response: Not available
- › If inductor current is too negative, highside FET may fail during the dead time between lowside off and highside on due to too much current going into the highside body diode.
- › NCL will set lowside to off once the inductor current reaches the negative current limit
- › To avoid chatting, the hysteresis level is set to release the HiZ only when the inductor reaches $\frac{1}{4}$ of the negative current limit and a minimum HiZ on time is satisfied.



Output Settings... limitations in OCP settings

- › There is a limitation in what values Avg OCP and OC Warning/PCC can have.
- › They can be set in steps of 2A and the range is 0-30A/phase less than Inst OCP.
- › When changing Inst OCP the AvgOCP and PCC will change the same amount. i.e. Change Inst OCP 7A and both other will also change 7A
- › InstOCP is not influenced by changes in AvgOCP or PCC
- › Example Inst OCP = 70A /phase AvgOCP = 60A and PCC = 46A
- › Change Inst OCP to 69A and that will make AvgOCP=59A and PCC=45A

Output Settings...

Avg OCP or Avg OC Warning behavior

Filter

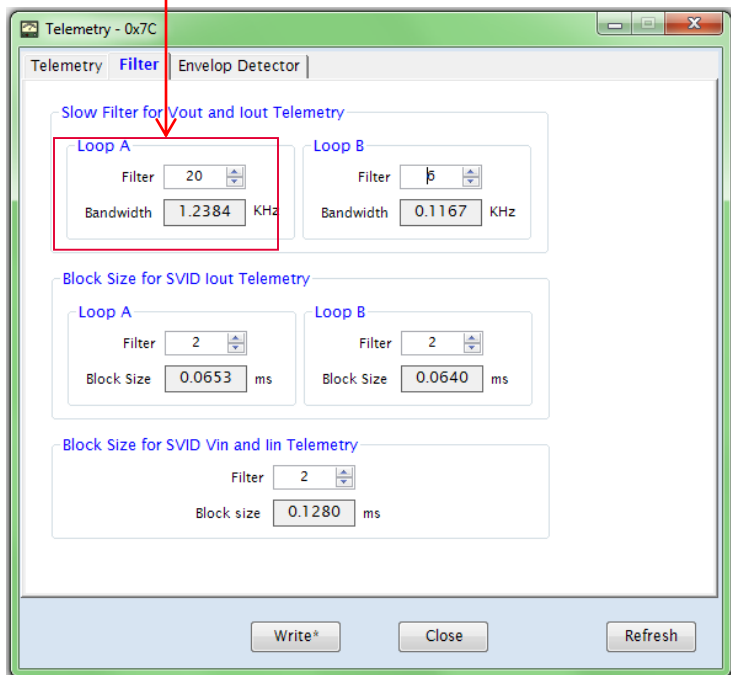
Filter frequency can be selected.

Time for a overcurrent signal to pass through the filter will depend on how much overcurrent.

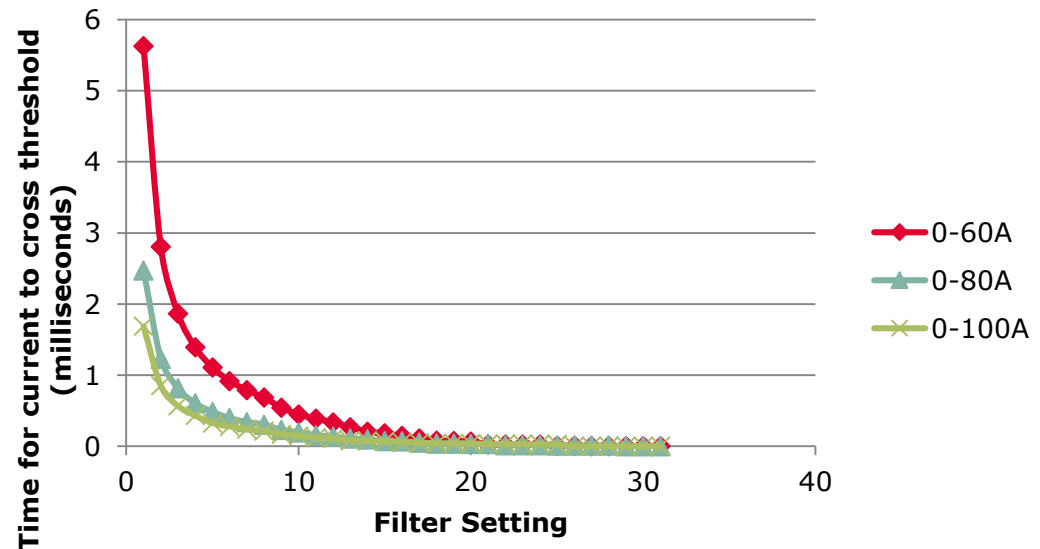
Like for any low pass filter a small current step take longer time to get to the threshold than a large overcurrent. See graph for example where limit is selected to 45A and different current steps.

Total delay times from an Overcurrent to fault response is the sum of Filter frequency selected and the corresponding delay time and also depend on switching frequency as there is an 5 consecutive sample digital delay after the filter. This digital delay makes higher filter frequencies insignificant to total time delay.

See block diagram on next page for more details.

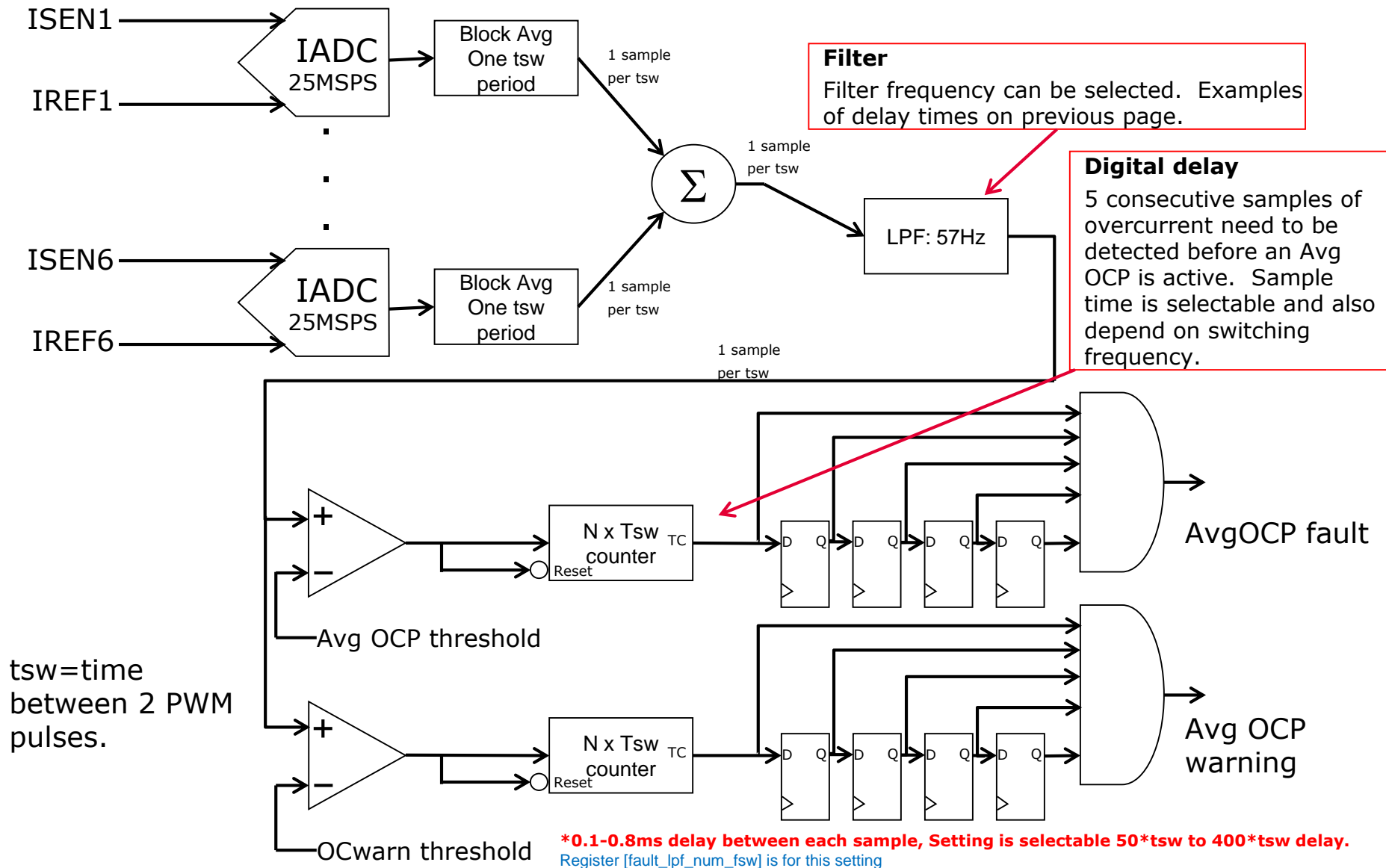


AVG OCP Low Pass Filter Time to cross a 45 Amp threshold

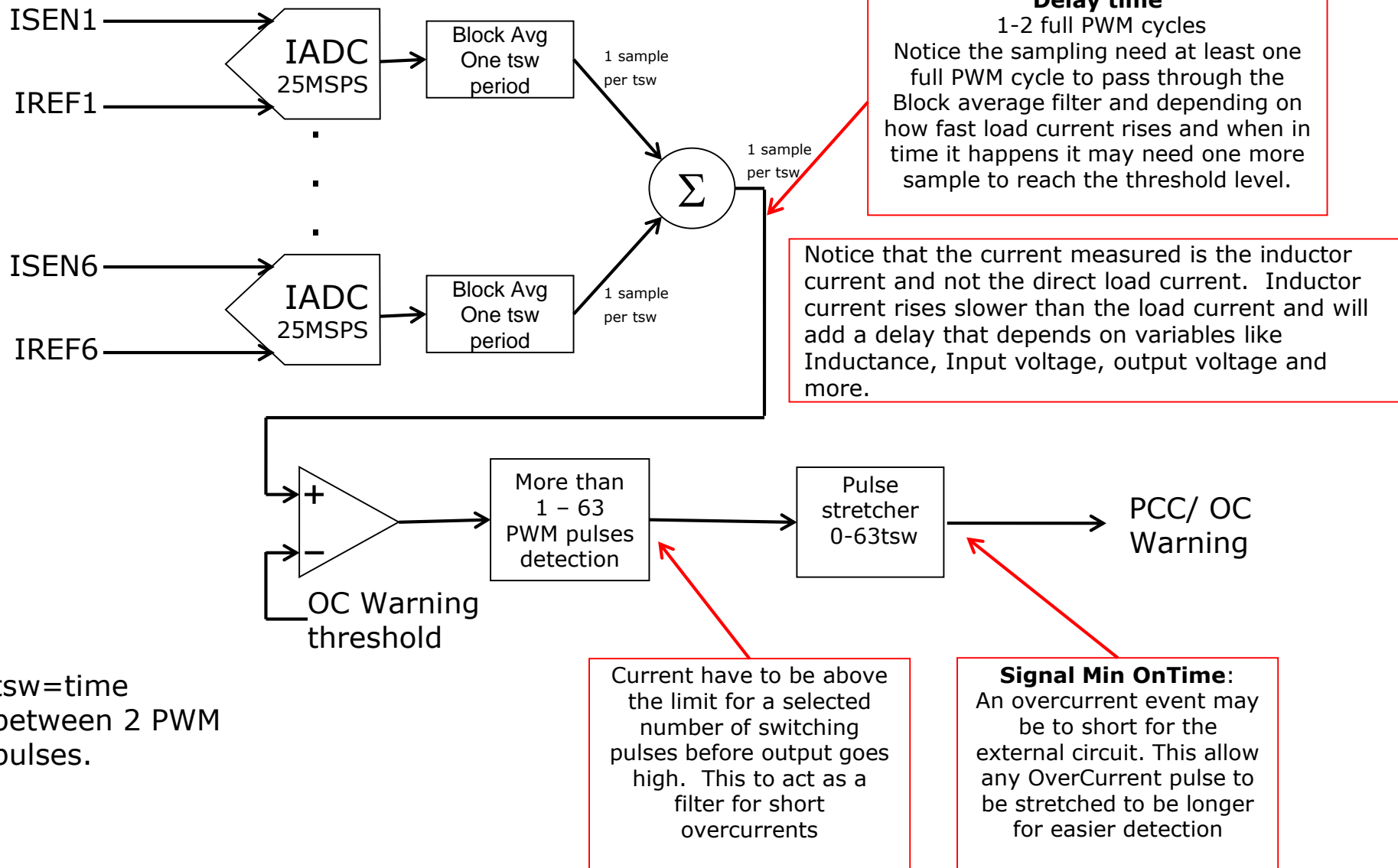


Output Settings...

Avg OCP and Avg OCP warning

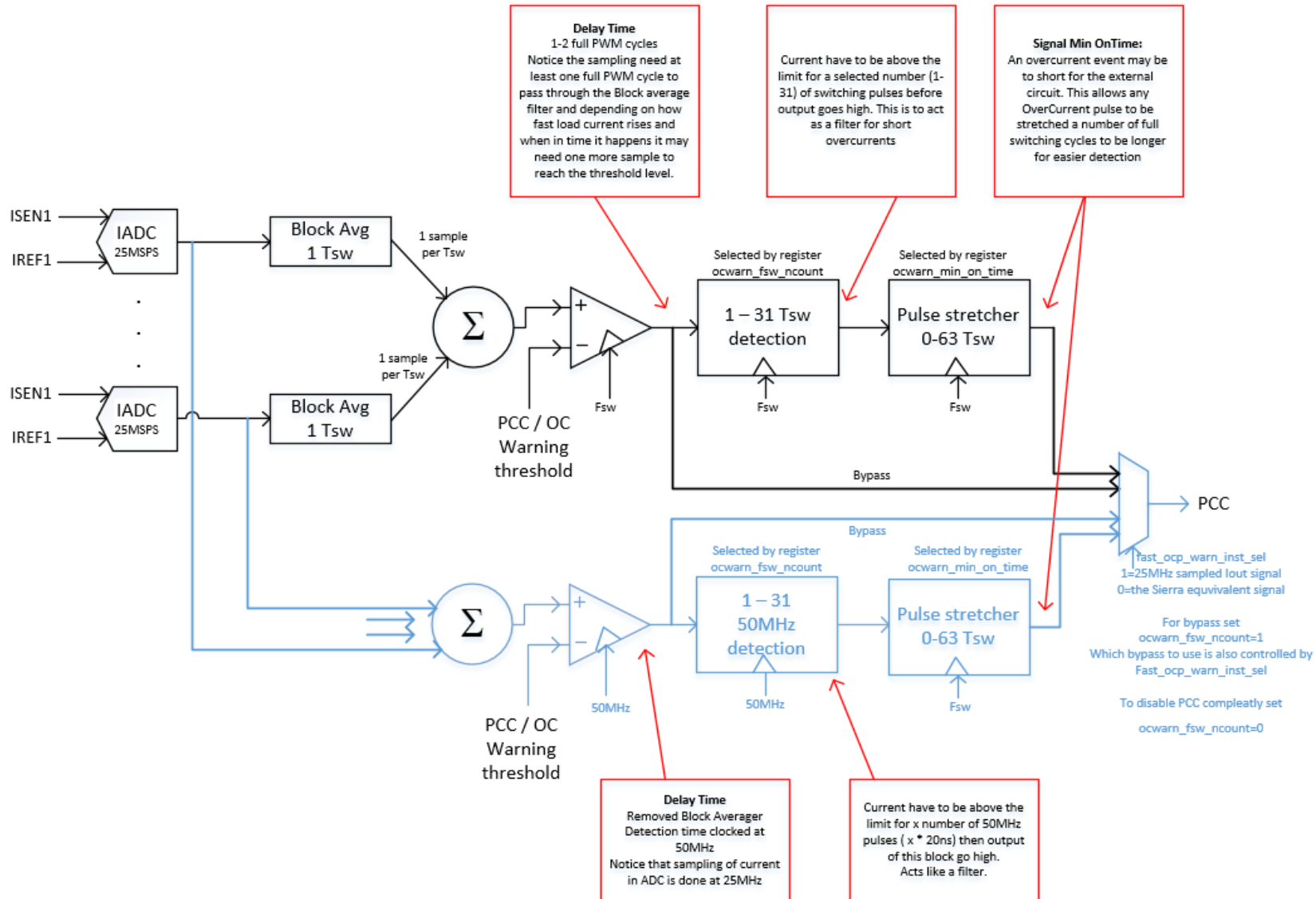


Fast OC warning Sierra and Sequioa Cycle sampling. AMD PCC peak current control

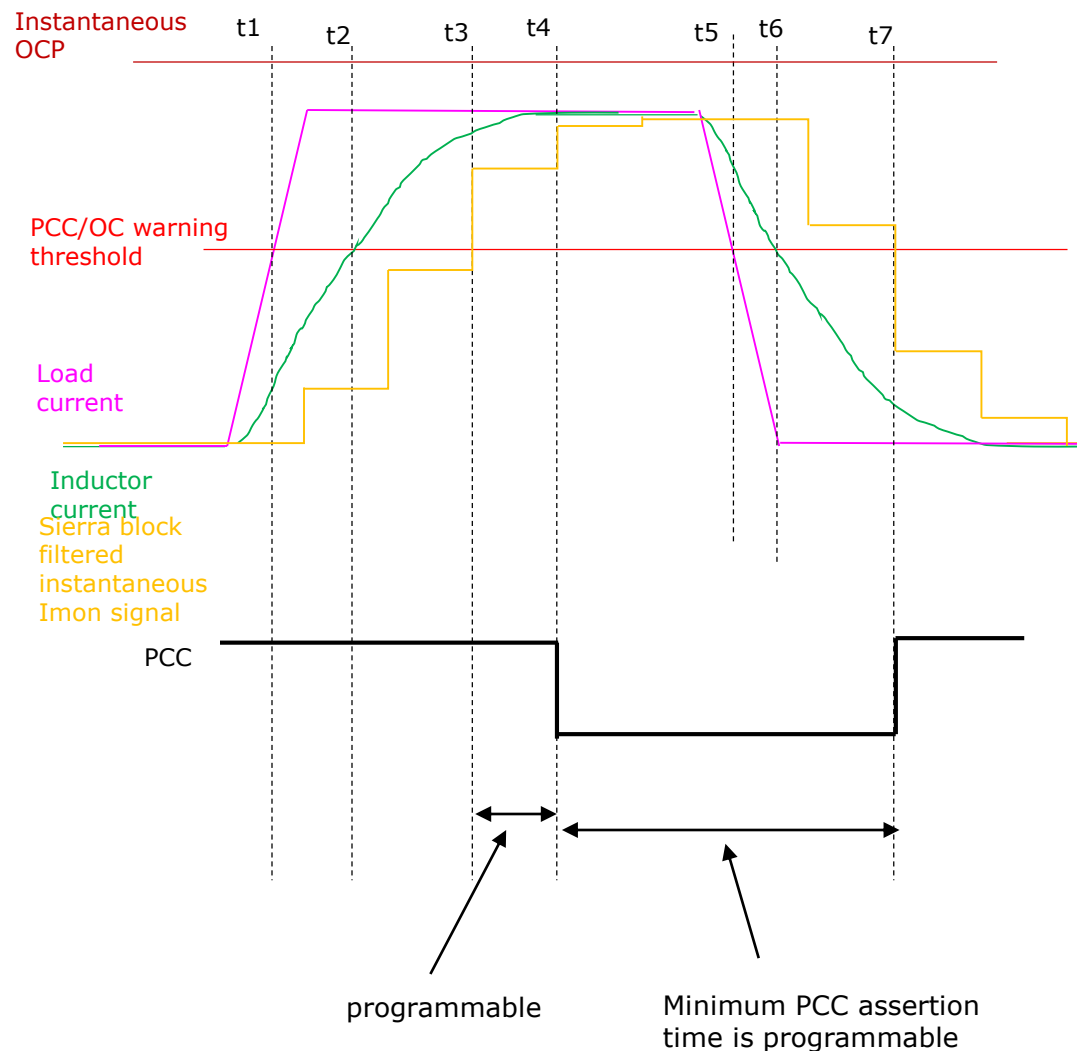


Fast OC warning Sequoia Inst. Current sampling

AMD PCC peak current control



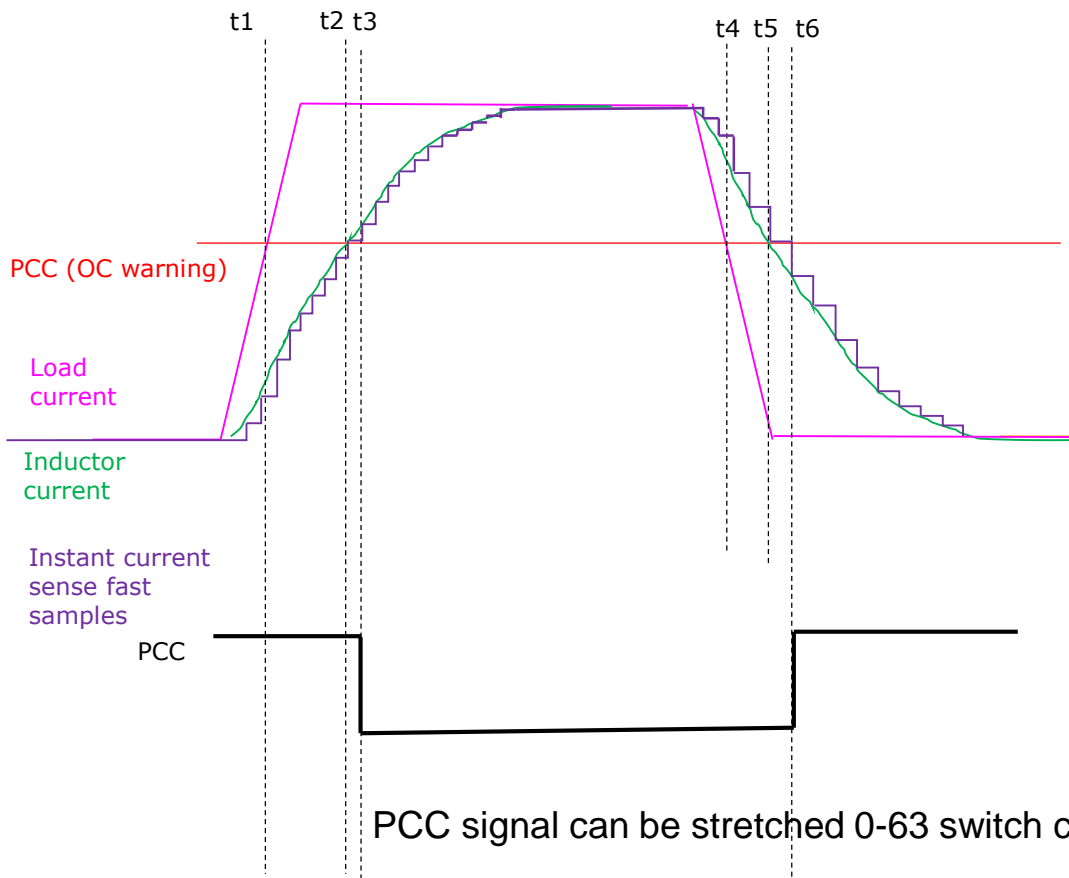
OC warning Sierra and Sequoia AMD PCC peak current control



- > t1: load current reaches OC warning threshold
Some of the current comes from the output capacitors while inductor current takes time to increase
- > t2: Inductor current reaches OC warning threshold. Contribution to the delay between t2 and t1:
 - Output inductance (Higher=slower)
 - Input voltage (higher=faster)
 - Loop bandwidth (higher=faster)
- > t3: Instantaneous Imon (switching cycle block averaged inductor current) reaches OC warning threshold. Delay between t3 and t2 is \leq two switching cycles
- > t4: PCC is asserted. Delay between t4 to t3 is programmable in range of 1~63 switching cycles
- > t5: load current decreases and reaches OC warning threshold
- > t6: Inductor current decreases and reaches OC warning threshold
- > t7: Instantaneous Imon follows inductor current and goes below OC warning threshold which de-assert PCC signal. Note: the assertion time should be $>$ minimum assertion time which is programmable in range from 0~63 switching cycles

Faster PCC only Sequoia XDPE142xx

AMD PCC peak current control



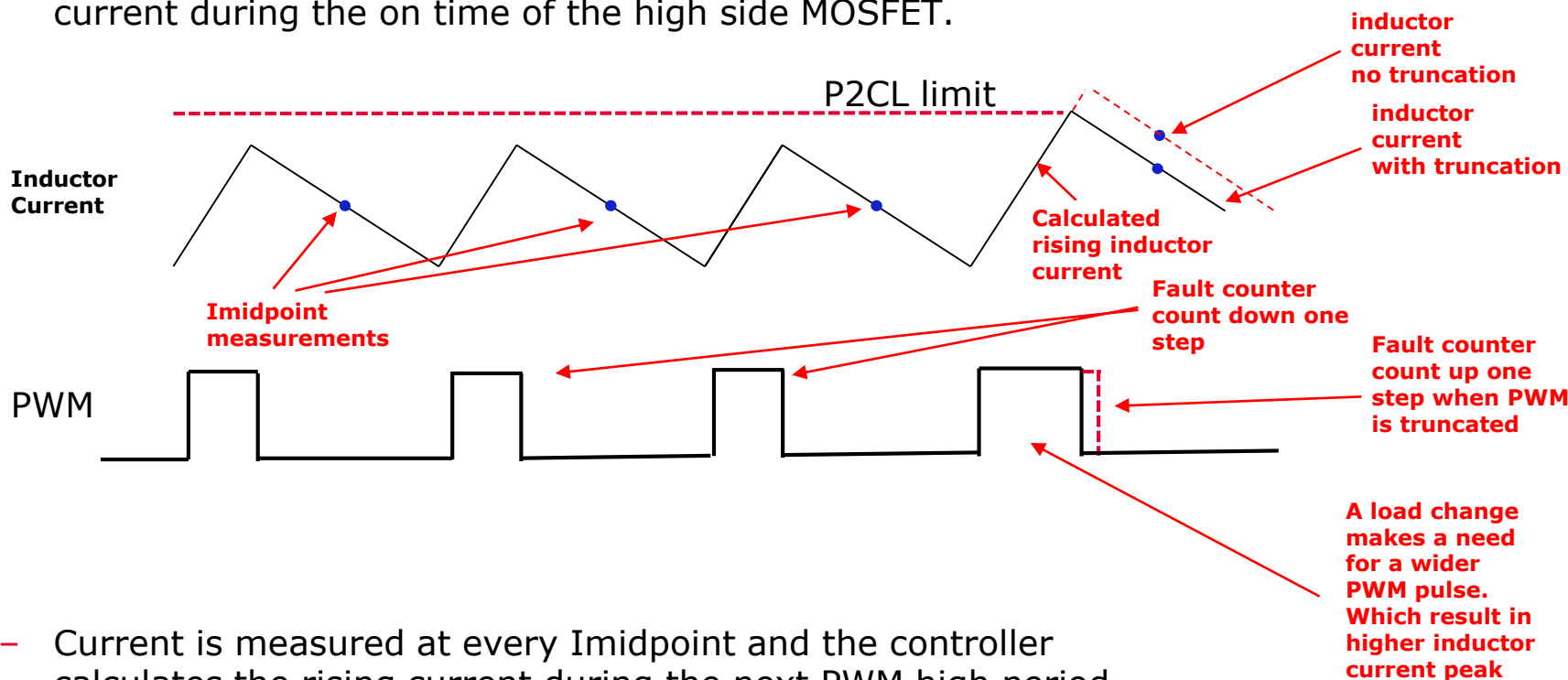
- › t1: load current reaches OC warning threshold
- › t2: Inductor current reaches OC warning threshold. Contribution to the delay between t2 and t1:
 - Output inductance
 - Input voltage
 - Loop bandwidth
- › t3: Current sampled at 25Mhz reaches OC warning threshold.
- › t4: load current decreases and reaches OC warning threshold
- › t5: Inductor current decreases and reaches OC warning threshold
- › t6: Current sampling follows inductor current and goes below OC warning threshold which de-assert PCC signal.

PCC signal can be stretched 0-63 switch cycles Shown with 0 stretch

P2CL Pulse to pulse cycle limit

› Internal Calculation of phase current

- Inductor value , Measured V_{in} , V_{out} and $I_{midpoint}$ are used to calculate the inductor current during the on time of the high side MOSFET.



- Current is measured at every Imidpoint and the controller calculates the rising current during the next PWM high period.
- When the calculated current reaches the P2CL limit the PWM will be truncated

P2CL Pulse to pulse cycle limit

Response :

- Each PWM pulse will immediately be truncated when the phase current exceed the P2CL limit
- Fault flagged after 255 switching cycles above limit.
It uses an up/down counter.
It will count down for all pulses that are below threshold and up again if new pulses exceed threshold.
When number of accumulated above threshold pulses reaches 255 a fault signal is generated.
- A single pulse under threshold will not reset counter to 0 like the other current limit functions
- Counter do not go below 0
- › Recommended settings: Inductor saturation current or 1-2A below saturation current
- › Shutdown response: Shutdown/Ignore/Hiccup